DEVI AHILYA VISHWAVIDYALAYA, INDORE

FACULTY OF ENGINEERING

SCHEME OF EXAMINATION
&
COURSE OF CONTENTS

M. E. (Electronics)
(Specialization in Digital Communication)

INSTITUTE OF ENGINEERING & TECHNOLOGY
(www.iet.dauniv.ac.in)

DEVI AHILYA VISHWAVIDYALAYA, INDORE
INSTITUTE OF ENGINEERING & TECHNOLOGY
ME. (Electronics Engineering) with specialization in Digital communication
Schemes of Subjects & Examination (Subject to revision)

Th Marks (Max 100, Min 50) shall be based on Theory paper-It shall be an examination in the end of the semester.
CW Marks (Max 50, Min 25) shall be based on Attendance (25), Marks obtained in Test-I & Test-II of 25 marks each. Average of the two tests will be taken for awarding the 25 marks.
SW Marks (Max 50, Min 25) shall be based on Attendance (25), Marks obtained in Two Experiments and Viva Voce (25)
Pr Marks (Max 50, Min 25) shall be based on Viva-Voce by External Examiner.

Th- Theory, CW – Class Work, SW – Sessional Work, Pr – Practical

Semester I

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5ET501	Advance Computer Networking	3	1	-	100	50	-	-	150
2.	5ET502	Embedded Microcontroller	3	1	2	100	50	50	50	250
3.	5ET503	Advance Digital Communication	3	1	2	100	50	50	50	250
4.	5ET504	Programming Language for Communication systems	3	1	2	100	50	50	50	250
5.		Elective-I	3	1	-	100	50	-	-	150
6.	5ET510	Comprehensive Viva-I	-	-	-	-	-	-	-	100
	TOTAL		**15**	**5**	**6**	**500**	**250**	**100**	**100**	**1150**

Semester II

SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5ET551	Modeling, Simulation and Evaluation Techniques	3	1	-	100	50	-	-	150
2.	5ET552	Advance Digital Signal Processing	3	1	2	100	50	50	50	250
3.	5ET553	VHDL for Communication Systems	3	1	2	100	50	50	50	250
4.	5ET554	Mobile Communication	3	1	2	100	50	50	50	250
5.		Elective-II	3	1	-	100	50	-	-	150
6.	5ET560	Comprehensive Viva-II	-	-	-	-	-	-	-	100
	TOTAL		**15**	**5**	**6**	**500**	**250**	**100**	**100**	**1150**

Elective – I: Any one of the following (I - Semester)

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5ET505	Advance Logic Design	3	1	-	100	50	-	-	150
2.	5ET506	Satellite Communication	3	1	-	100	50	-	-	150
3.	5ET507	Software Engineering	3	1	-	100	50	-	-	150
4.	5ET508	Optical Communication Networks	3	1	-	100	50	-	-	150
5.	5ET509	Web Technology	3	1	-	100	50	-	-	150

Elective – II: Any one of the following (II - Semester)

SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5ET555	Multimedia Communication	3	1	-	100	50	-	-	150
2.	5ET556	Fuzzy Logic & Neural Network	3	1	-	100	50	-	-	150
3.	5ET557	Network Security	3	1	-	100	50	-	-	150
4.	5ET558	Broadband Communication	3	1	-	100	50	-	-	150
5.	5ET559	VLSI Technology	3	1	-	100	50	-	-	150

Semester III

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	6ET501	Dissertation Phase-I	-	-	8	-	-	100	50	150
	TOTAL		**-**		**8**	**-**	**-**	**100**	**50**	**150**

Semester IV

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	6ET551	Dissertation Phase-II	-	-	12	-	-	250	100	350
	TOTAL		**-**		**12**	**-**	**-**	**250**	**100**	**350**
		GRAND TOTAL OF FOUR SEMESTERS								**2800**

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET501 Advance Computer Networking	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
Appreciate working network layer protocols, selection of appropriate routing algorithm, understanding of QOS parameters, understanding of transport and application layer protocols, use of cryptography in computer networking.

Prerequisite(s):
Fundamentals of computer networking, concepts of programming and operating systems.

COURSE OF CONTENTS

UNIT -I
Introduction and overview of OSI reference model, TCP/IP reference model, physical layer and its functions, data link layer, MAC sub layer, their functions, overview of data link layer and Mac sub layer protocols (stop & wait, sliding window, aloha, CSMA, CSMA/CD, CSMA/CA).

UNIT -II
Network layer Design Issues, Routing Algorithms Shortest Path Routing, Flooding, Distance Vector Routing, Link State Routing, Broadcast Routing, Multicast Routing, and Routing in Ad Hoc Networks. Congestion Control Algorithms, General Principals , Prevention Policies, Congestion Control in, Virtual Circuit Subnets, Datagram Subnets, Load shedding, Jitter Control.

UNIT -III
Quality of Services, Requirements, Techniques for Achieving Q OS, Internetworking, Tunneling, and Internet work Routing, Network Layer in the Internet, IP Protocol, IP Addresses, OSPF, BGP, Internet Multicasting, Mobile IP IPV6.

UNIT -IV
Transport Service, Services Provided to Upper Layers. Transport Primitives, Berkeley Sockets, Elements of Transport Protocols, Addressing, Introduction to UDP, Introduction to TCP, TCP Service Model, TCP Protocol, TCP Segment Header. Performance Problems in Computer Networks , Network Performance Measurements. System Design for Better Performance.

UNIT -V
Various Application Layer Protocols DNS, SMTP, IMAP, WWW,
Introduction to Cryptography, Substitution Ciphers, Transposition Ciphers, Symmetric and Asymmetric Key Algorithms, DES, RSA, Digital Signature.

BOOKS RECOMMENDED
[1] A. S. Tanenbaum, *"Computer Networks",* 4th Edition Pearson Education, 2003.
[2] W. Stalling, *"Network Security and Cryptography",* 4th Edition Pearson Education, 2006.
[3] W. Stalling, *"Data & Computer Communication",* 8th Edition Pearson Education, 2006.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET502 **Embedded Microcontroller**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
Designing microcontroller hardware, understanding use of timers and interrupts in different applications ability to serially transmit-receive the data at standard baud rate with an interface, using microcontroller in industrial applications, embedded software architecture

Prerequisite(s):
Knowledge of microprocessor, peripherals, interfaces and assembly language programming

COURSE OF CONTENTS

UNIT -I
Microprocessor and microcontroller comparison, microcontroller survey, 8051 architecture General purpose registers, special function registers, input/output ports and circuits, internal memory connecting external memory, and I/O interface 8255 ,data transfer, arithmetic, logical, branch instructions, bit-related instructions , assembly language programming

UNIT -II
Interrupts ,timer flag interrupt , serial port interrupt ,external interrupt ,interrupt control, interrupt priority interrupt destination , software generated interrupts , counter and timers , timer modes of operation ,timing subroutines-pure software time delay, software polled timer, pure hardware delay, look-up tables

UNIT -III
Serial data communication, different modes , serial data transmission-reception using time delay , by polling , interrupt driven , microcontroller applications as interfacing with keyboard and display devices A/D and D/A converters , waveform generation , frequency and pulse width measurement, stepper motor control etc.

UNIT -IV
8051 family members as 8052 with capture timer, A/D and D/A equipped family members, watch dog timer, pulse width modulation, analog comparators, PIC 16C6X/7X,16 F8XX microcontroller and architecture , industrial applications of microcontroller

UNIT -V
Software architectures-Round robin, Round robin with interrupts, function-queue-scheduling, Real time operating system architecture – task states, scheduler, reentrancy, shared data problem, interrupt latency RTOS-semaphores and problems , inter - task communication with message queues, mailboxes and pipes,
Basic design using real time operating system

BOOKS RECOMMENDED

[1] Mohamed. Ali Mazidi, Janice Ali Mazidi, Rolin D. McKinley, *"The 8051 microcontroller &r Embedded System*, 2nd Edition Pearson Education, 2006
[2] Kenneth J.Ayala, *8051 microcontrolle r*, Architecture*, Programming & Applications,* Penram international publishing (India) Pvt Ltd, 1996
[3] David E. Simon, *An Embedded software Primer*, Ist Pearson education, 1999

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I - SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET503 Advanced Digital Communication	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:

To give exposure of all the processes like modulation, Demodulation, Channel Coding, Decoding etc. of physical layer involved in modern telecommunication systems like in Mobile communication, Wireless Local area Networks.
To develop skills to analyze these processes using basic Fourier techniques.
To evaluate performance of a digital communication system using the Matlab function.
To develop an orientation towards research in telecommunication engineering.

Prerequisite(s):

Basic knowledge of digital communication.

COURSE OF CONTENTS

UNIT -I

Review of Fourier Techniques and its application for Linear System analysis, Fourier Transform Properties, Classification of Signals, Spectral Density, Autocorrelation, Random Signals (random Variables, Random Processes, Stationarity, Time Averaging and Ergodicity), Noise in Communication Systems, Bandwidth of Digital Data.

UNIT -II

Formatting and baseband Modulation and Demodulation - Sampling & quantization, Non uniform Quantization, Digital Encoding Techniques, PCM, DPCM, ADPCM, DM, ADM,Line Coding NRZ, RZ, Bi phase, Duo binary etc., their comparison and Spectrum associated with their waveforms, Detection of Binary Signals in Gaussian Noise, Maximum Likelihood Receiver Structure, Matched filter, Correlator, Error Probability Performance of Binary signaling, M'ary Pulse Modulation, Pulse Shaping, Duo-binary Signaling, Eye Patterns.

UNIT –III

Band Pass Modulation and Demodulation- Digital Band pass Modulation Techniques binary PSK, DPSK, QPSK, M-ary PSK, QAM, M-ary FSK, MSK, GMSK their Generation, Signal Space representation, Band-width requirements, Detection (Coherent, Non-coherent), Performance analysis and Comparison in presence of noise.

UNIT –IV

Selected topics in Digital Communication- Digital transmission in Fading Multipath Channels, Types of Fading, Mitigating the Effects of Fading, Spread Spectrum Communication Systems, Generation of PN Sequences, Direct Sequence Spread Spectrum, Frequency Hopped Spread Spectrum, Its applications to communication systems, Multi Carrier Modulation and OFDM, An OFDM system Implemented via FFT Algorithms, Application of OFDM.

UNIT –V

An Introduction to Information Theory, The Source Coding Theorem, Huffman and Lempel-Ziv Source Coding Algorithms, Modeling of Communication Channels, Channel Capacity, Bounds on Communication, Types of Error Control, Linear Block Codes, Generator Matrix, Parity Check Matrix, Error Correction and Syndrome Testing, Minimum Distance of a Linear Code, Cyclic Codes, Hamming Codes, BCH Codes, Convolutional Encoding, State, Tree, Trellis Diagram, Maximum Likelihood Decoding, Hard and Soft decisions, Properties of Convolutional Codes, Finite Fields, R-S Coding and Decoding, Introduction to Interleaving and Concatenated Codes.

BOOKS RECOMMENDED

[1] Bernard Sklar, "*Digital Communication*", Pearson Education, 2nd Edition, 2004.
[2] J.G.Proakis & M.Salehi, "*Fundamentals of Communication Systems*", Pearson Education, 2006.
[3] J.G.Proakis, *Digital Communication*, McGraw Hill, 4th Edition, 2001.
[4] Taub & Schilling, *Principles of Communication System*, 2nd Edition, TMH
[5] Lathi B. P., *Modern Analog and Digital Communication Systems*, 3rd Edition, Oxford Univ. Press,.
[6] Haykins Simon, *Digital Communication*, 3rd Edition, Wiley Publication.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I - SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET504 Programming Language for Communication Systems	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
To understand and learn a programming language that expressly designed for use in the distributed environment of the technology along with an object-oriented programming model.

Prerequisite(s):
Knowledge Object Oriented Programming concept using object oriented languages such as C++, Objective C, Smalltalk, Eiffel, Common LISP Object System (CLOS), Object Pascal, and ADA 95 etc.

COURSE OF CONTENTS

UNIT -I Introduction to Object Oriented Programming and Java :
Object Oriented Concepts, Abstraction, Encapsulation, Information Hiding. Java features: Java syntax, data types, data type conversions, control statements, operators and their precedence. Introduction to Class: Instance members and member functions. Concept of object initialization, constructors, constructor overloading. Access modifiers: Class attributes and methods

UNIT -II
Inheritance and Polymorphism
Class relationships: Inheritance and its types, Merits and Demerits, Polymorphism: Dynamic method dispatch, Runtime polymorphism, Abstract classes, Interfaces and packages.

UNIT -III
Exception Handling, Multithreading and Introduction to Java APIs:
Exceptions: Need for exceptions, Checked V/s Unchecked exceptions, creating exceptions.
Multithreading: Introduction, Priorities and scheduling, Thread Synchronization and its life cycle. String Handling, Wrapper classes: Arrays and Vectors

UNIT -IV
Java I/O, Applets and Event Handling:
Basic concept of streams I/O stream & reader-writer classes. File handling. Applet and its Life Cycle,
Basic GUI elements, Event Delegation Model and event handling

UNIT -V
Introduction to elementary procedures, Real & Complex vector and Matrix & Determinants and operations like: Initialization, Duplication, Elimination, Interchanging, Rotation, Norms, Scaling, Multiplication & calculation of rank etc.
Evaluation of various polynomials like Chebyshev polynomial, Fourier polynomial etc.
Analysis of real matrix problems like: Overdetermined systems, underdetermined system, homogenous, pseudo inversion. Sparse Real matrices, Similarity Transformation, Eigen value problems.
Numerical differentiation, Differential equations,
Introduction to special functions like: Exponential, Gamma, Error, Infinite time series, Fast Fourier transforms etc

BOOKS RECOMMENDED
[1]Hang T. Lau, *A Numerical Library in Java for Scientist & Engineers*, Library of Congress Cataloging-in-Publication Data by Chapman & Hall/ CRC Press Company.
[2] Cay S.Horstmann, *Core JAVA Vol-1*, Pearson Education.
[3] Herbert Schildt, *The complete Reference,* Tata McGraw Hill
[4] Kathy Sierra, *Bert Bates, Head First Java,* 2nd Edition, Oreilly

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I – SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET505 (Elective)	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
Advanced Logic Design	**3**	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objective:
To provide an in-depth knowledge regarding designing of advance digital circuits. To emphasize on FSM based sequential circuit design and analysis of designed circuits for timing and performance.

Prerequisite:
Knowledge of basic digital electronics and state diagrams.

COURSE OF CONTENTS

Unit-I
Background for Digital Design
Logic Function Representation and Minimization, K-Map Minimization,EV- K-Map Minimization, Function Minimization by Using K-map XOR Patterns and Reed-Muller Transformation

Unit-II
Combinational Logic Design
No arithmetic Combinational Logic Devices –Multiplexers, Decoders, Encoders, De-Multiplexers, Code Converters, Magnitude Converters, Parity Generators and Error Checking Systems, Combinational Shifters, Steering logic and Tri-state gate application.
Arithmetic Devices – Binary adders and substractors, Carry Look ahead Adder, Multiple -number addition and Carry save adder, Multipliers, Parallel Dividers, Dedicated ALU design featuring RC and CLA Capability, Mux approach to ALU Design, Dual Rail system and ALU with completion signals.
Propagation Delay and Timing Defects in Combinational Logic.

Unit-III
Introduction to Synchronous State Machine Design and Analysis
Models for Sequential Machines, Basic Memory Cell, Flip-flop, Flip-Flop Conversions, Asynchronous Preset and Clear overrides, Latches and Flip-flop Timing Problems, Design of Synchronous state machine, Detection and elimination of output race glitches, static hazard in output logic, Clock Skew, Switch debouncing circuit, ASM chart and state tables.
Module and Bit-Slice Devices- Registers, Synchronous binary counters, Shift register counters, Asynchronous counters.

Unit-IV
Asynchronous State Machine Design and Analysis
Features of Asynchronous FSM, Lumped path delay models, Excitation table for LPD model, State diagram, state table and excitation table for Asynchronous FSM, Basic cell design using LPD model, Design of RET Flip-flops, Detection and elimination of timing defects, single transition time machines, Hazard free design, One Hot Design for asynchronous FSM.

Unit-V
Advance Sequential Designs
Externally Asynchronous/ Internally Clocked systems and Applications, Asynchronous Programmable Sequencers, One –hot Programmable asynchronous sequencers, Pulse mode approach to asynchronous FSM Design.

Books Recommended:

[1] Richard.F.Tinder, "*Engineering Digital design"*, 2nd Edition, 2000, Academic Press.
[2] William I. Fletcher, " *An Engineering Approach to Digital Design* " , Prentice Hall of India, 1996.
[3] James E. Palmer, David E. Perlman, *" Introduction to Digital Systems* ", Tata McGraw Hill, 1996.
[4] N.N. Biswas, *" Logic Design Theory* ", Prentice Hall of India, 1993.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I – SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET506 Satellite Communication	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Paper: 3 Hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
This course consists of three parts. The first part addresses the satellite systems covering the topics of orbits and constellations, satellite space segment, and propagation and satellite links. The second part reviews satellite communications techniques including modulation, coding, multiple access and on-board processing. The third part presents various satellite communications systems and applications with emphasis on recent development in LEO satellite systems for personal communications.

Prerequisite(s):
Radio Propagation , Electromagnetic Theory, Antenna and Wave Propagation.

COURSE OF CONTENTS

Unit-I
Introduction: Satellite system architecture, factors influenced the system, Satellite orbits, Classification of Orbits, Orbital Perturbations, Orbital Maneuvers, Satellite Constellations.

Unit-II
Radio Link: The basic RF link, Link Equation, Link Performance, Satellite links: Up link Equation and Down link equation, Overall system Performance.

Unit-III
Modulation, Coding and Multiple Access: Source Signals- Voice, Data and Video, Analog transmission system, Digital transmission system and TV transmission system, Coded orthogonal frequency division multiplexing (COFDM) modulation system.

Unit-IV
Multiple Access: Basic multiple access resources, Multiple access format, FDMA, Preassigned and Demand assigned FDMA, TDMA system, TDMA frame structure, TDMA terminal equipment, Satellite switch TDMA, CDMA, Spread spectrum technique, Direct and Frequency Hopping CDMA.

Unit-V
Commercial issue and Applications: Transponders, Satellite navigation system, Direct Television Broadcast system, VSAT system, GPS system.

BOOKS RECOMMENDED:
[1] M. Richharia,"*Mobile Satellite Communications*", 2nd Edition, Pearson Education Asia, 2004
[2] T. Pratt, C. Bostian and J. Allnutt,"*Satellite Communications*" John Wiley and Sons, 2003.
[3] W. Pritchard, H. Suyderhoud and R. Nelson, "*Satellite Communication System Engineering*", 2nd Edition, Pearson Education Asia, 2005
[4] D. Roddy, "*Satellite Communication*", 3rd Edition , McGraw-Hill, March 2001.
[5] Bruce R. Elbert, "*Introduction to Satellite Communication*", 2nd Edition, Artech House, Inc, 1999.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication) I – SEMESTER					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET507 (Elective) Software Engineering	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory Paper: 3 Hours				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objective:
To familiarize with the process of software development life cycle using the concepts of software engineering.

Prerequisites:
Knowledge of a programming language, preferably object oriented and a midsize project work

COURSE OF CONTENTS

Unit I
Software Engineering Process- Basic concepts of Software Engineering; Software life cycle; Role of Software Engineer; Application Domains, System Engineering; Software Quality.

Unit II
Software Design – Concepts of Analysis and Design; Object Orientation; Object Oriented Design; Design Issues; Case Studies.

Unit III
Verification and Validation – Testing; Debugging Analysis; Software Testing Strategies; Software Metrics.

Unit IV
Software Engineering Process Models - Different Models; Process Organization; Management planning control, Organization and Risk Management.

Unit V
Software Engineering Tools – System Programs, Role of Programming languages; CASE Tools; Objected Oriented Software Engineering; Reengineering process ,Client Server Software Engineering.

BOOKS RECOMMENDED:

[1] C.Gezzi, M. Jazayeri and D. Mandriohi *Fundament of software Engineering*, PHI 1996.
[2] R.S. Pressman, *Software Engineering A Practitioner Approch*, 4th Edition, Mcgraw Hill International Edition 20070
[3] P.Jalote, *An Integrated Approach to Software Engineering,* Naresa Publishing, latest Edition.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET551 Modeling Simulation and Evaluation Techniques	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:

- To give exposure of stochastic processes and to show their importance in engineering education and research
- To develop skills to identify a process, its inputs and outputs. Then to develop a model and quantify the results.
- To give an hands on experience in MATLAB to be used as a simulation tool for the stochastic processes
- To develop an orientation towards research in electronics and computer engineering.

Prerequisite(s):
Fundamental knowledge of Probability Theory.

COURSE OF CONTENTS

UNIT –I
Introduction to Probability Theory - Relative Frequency and Classical Definitions, Sample Space and Events, Conditional Probabilities, Independent Events, Bayes Formula, Bernoulli Trials.

UNIT –II
Random Variables - Definition, Discrete and Continuous Random Variables, Cumulative Distribution Function(CDF), Probability Density Function (PDF), Distributions for Discrete and Continuous Random Variables, Geometric Distribution, Poisson Distribution, Uniform Distribution, Exponential Distribution, Normal Distribution, Mean, Variance and Moments of Random Variables, Function of a Random Variable and it's Expectation, Jointly Distributed Random Variable, Moment Generating Function.

UNIT –III
Markov Chains- Classification of Stochastic process, Introduction to Markov chains, Classification of States, Transition Probabilities, Limiting State Probabilities, Higher Transition Probabilities, and Chapman Kol Mogorov Equation, Concept of Transient States and Absorption Probabilities, Solution of Problems Based on Markov Chains.

UNIT –IV
Markov Processes and Queuing Theory-Introduction to Continues Time Markov Chains, Birth and Death Processes, The Transition Probability Function, Limiting Probabilities, Non Birth Death Processes, Exponential Distribution & Poison Process. Solution of Problems Based on Continuous Time Markov Chains, Introduction to Queuing Theory and M/G/1 Queuing Systems.

UNIT –V
Simulation- Simulation of Queues, Statistical Inference and Few Examples on Simulation.

BOOKS RECOMMENDED

[1] K.S.Trivedi*, "Probability and Statistics with Reliability, Queuing and Computer Science Applications*", 2nd Edition , A Wiley-Interscience Publication.
[2] Averill M. Law, W. David Kelton, "*Simulation Modeling and Analysis*"**,** 3rd Edition**,** Tata McGraw-Hill Publication.
[3] S.M. Ross, "*Introduction to Probability Models***,** 9th Edition**,** Elsevier Publication", 2007.
[4] A Papoulis, S.V Pillai, "*Probability Random Variables and Stochastic Processes*", 4th Edition, TMH Publication, 2002.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET552 **Advance Digital Signal Processing**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objective:
To provide clear conceptual knowledge of different DSP algorithms and to introduce speech, multimedia and other signal processing applications.

Prerequisite(s):
A basic course in Digital signal processing.

COURSE OF CONTENTS

UNIT -I
Signals and Signal Processing: Characterization and Classification of signals; Sampling and Quantization; Typical signal Processing Operations; Examples Typical Signals and Systems; Typical Signal Processing applications; Why Digital Signal Processing; Building blocks of a Digital signal processor; Discrete Time Fourier Transform, Z – transform and properties.

UNIT -II
Discrete Fourier Transform: Introduction; Computation of DFT and IDFT; Periodic and symmetry properties of DFT; DTFT v/s DFT; Circular shift and Circular convolution Linear convolution using DFT; Block convolution, Overlap – add method and Overlap – save method.

UNIT -III
Fast Fourier Transform: Redix Two DIT and DIF FFT algorithm; Butterfly computation; Bit reversed mapping; In place computation; Composite – N algorithm; Prime factor algorithm.

UNIT -IV
Digital Filter Structures: Block Diagram Representation; Signal Flow Graph Representation; Equivalent structures; Basic FIR Digital Filter structures; Basic IIR filter structures; state space structure; All Pass Filter; Tunable HR Digital filters; Cascaded lattice realization of IIR and FIR Filters; Parallel all Pass Realization of IIR Transfer Function; Computational Complexity of Digital Filter structures; Tellegen theorem and its applications.(Transposition theorem and Network sensitivity formula.)

UNIT -V
Digital Filter Design: Brief Review of Analog Filter Design; Impulse Invariance method of IIR filter design; bilinear Transform Method of IIR Filter Design; Design of Digital HR notch Filters; Low Pass HR digital filter design based on Truncated Fourier Series; FIR Filter Design Based on Frequency Sampling Approach; computer aided design of digital filters. Introduction to speech and language processing.

BOOKS RECOMMENDED

[1] Sanjit K. Mitra; *Digital Signal Processing A Computer- Based Approach*; 9th Edition, Tata McGraw Hill .
[2] V.K.Khanna;*Digital Signal Processing; Telecommunications and Multimedia Technology* Wheeler Publishing 1999.
[3] Richard G. Lyons Understanding *Digital Signal Processing*; .; First Indian Reprint ,Addison Wesely Longman Inc 1999.
[4] B. Somanathan Nair "*Digital Signal Processing, Theory, analysis and Digital filter design"*; PHI New Delhi India 2005.
[5] A. V. Oppenheim and R. W. Schafer "*Digital Signal Processing"*

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET553 VHDL for Communication Systems	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
To enable the students to translate a functional system description into appropriate digital blocks coded in VHDL .Perform synthesis, place, and route of a digital design into a target FPGA

Prerequisite(s):
Digital Design, Microprocessor architecture, C++ language.

COURSE OF CONTENTS

UNIT –I
Introduction to VLSI
History of IC Design, IC Technology, Moore's Law, IC Design Constraints, Feature Size, VLSI Family, Programmable Logic Devices, Designing with Programmable Logic- Design Entry, Simulation, Synthesis, Implementation, Device Programming, EDA Tools, IP Cores, Gjeski's Y Chart.

UNIT -II
FPGA and CPLD
ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array (LCA) – I/O Block – Programmable interconnect – Xilinx – 3000 series and 4000 series FPGAs. Altera CPLDs, altera FLEX 10K series PLDs.

UNIT -III
Introduction to VHDL
Digital system design process , Hardware simulation , Levels of abstraction , VHDL requirements , Elements of VHDL Top down design, VHDL operators ,Timing ,Concurrency ,Objects and classes , Signal assignments ,Concurrent and sequential assignments.

UNIT -IV
Modeling Techniques and Advance Topics
Entity Declaration, Architecture Body, Process statement, Loop control statements, Multiple Processes, Delay Models, Signal Drivers, Block statements, Component declaration and Instantiation, Concurrent Assignment statements, Generics and Configuration, Subprogram, Overloading, Packages and Libraries, Design Libraries, Generate statements, Attributes, Hardware Modeling Examples: Modeling of digital modulator and demodulators, digital filters, WAP protocols, network security modules, wireless signal reception modules etc.

UNIT -V
Design for Synthesis
Language directed view of synthesis, Inference from CSA statements, Inference from within Process, Inference using Signals v/s variables, Latch v/s Flip Flop Inference, Wait statements, Synthesis Hints.

Text
1. J. Bhasker, "*VHDL*", 3rd Edition, Addison Wesley, 1999.

BOOKS RECOMMENDED
[1] P.K. Chan & S. Mourad, "*Digital Design sing Field Programmable Gate Array*" 1st Edition, Prentice Hall, 1994.
[2] J. V. Old Field & R.C. Dorf, "*Field Programmable Gate Array*", John Wiley, 1995.
[3] M. Bolton, "*Digital System Design with Programmable Logic*", Addison Wesley, 1990.
[4] Sudhakar Yalamanchili, "*Introductory VHDL- From Simulation to Synthesis*", 3rd Indian Reprint., Pearson Education,
[5] Douglas Perry, "*VHDL*", 3rd Edition, McGraw Hill 2001.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET554 – Mobile Communication	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
To provide the knowledge of different generation mobile communication system, cellular concept, and the aspects of mobile radio environment which is very different than conventional communication system.

Prerequisite(s):
It is expected to know the following concepts: Electromagnetic spectrum, analog and techniques, Shannon Fano & Huffman coding, Channel coding theorem, Codes.

COURSE CONTENTS

UNIT -I
Introduction to wireless communication system. Conventional mobile system, Concept of cellular mobile system, Frequency Management Channel assignment, Co channel interference reduction, Handoff strategies and considerations, Cell capacity, Cell splitting, Sectorization of cells, Micro cell zone concept. Trunking and grade of service.

UNIT -II
Duplexing techniques, Comparison of FDMA and TDMA mobile systems, Principles of CDMA mobile system, Packet radio protocols.mobile radio propagation: Large scale path loss, Free space propagation model. Three basic propagation mechanism: Reflection, Diffraction, Scattering, Practical Link Budget design using path loss models, Outdoor propagation models. Small scale fading and multipath.

UNIT -III
Modulation Techniques for mobile radio, Equalization Techniques Diversity Techniques. RAKE Receiver, Channel coding, Speech coding technique.

UNIT -IV
Wireless system and standards: GSM system and architecture CDMA network (IS-95) : Architecture, Forward link, Reverse link, IEEE 802.11 standard, IEEE 802.16 Standard, WCDMA, CDMA 2000. DECT standard, Architecture and protocols. Up gradation for GSM:- HSCD, GPRS, EDGE.

UNIT -V
Mobile Network layer, Mobile transport layer, WAP, air interface, system development, mobile management, radio resource management, EIRP management, radio frequency monitoring, Quality of service, Mobile satellite system.

BOOKS RECOMMENDED
[1] TS Rappaport *"Wireless Communication"* ,Pearson Education
[2] Jacohen Schilling "*Mobile Communication"*, Pearson Education

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET559 VLSI Technology	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
This course presents the fundamental of CMOS VLSI design with different VLSI design methodologies and combinational, sequential and semiconductor memory circuit design. It also covers the limitations of CMOS in NANO technology with introduction to the NANO Technology

Prerequisite(s):
Knowledge of semiconductor devices is required.

COURSE OF CONTENTS

UNIT -I
Introduction: VLSI design flow, VLSI design style, Fabrication process Flow: basic Steps, the CMOS n-well Process.
Metal oxide semiconductor (MOS) structure, Types of MOSFET: Enhancement and Depletion. Structure and operation of MOS transistor. MOSFET process simulation.

UNIT -II
MOS transistor: threshold voltage of MOSFET, controlling of threshold voltage, MOSFET current – Voltage Characteristics. Transconductance, Drain conduction. Aspect ration, process parameters, second order effects, MOS small signal and Large signal model, MOS capacitances.

UNIT -III
CMOS Inverter: Analysis of different types of inverter circuit, CMOS inverter, transfer characteristic, calculation of propagation delay, rise time, fall time, noise margin and power dissipation for CMOS Inverter. Effect of threshold voltage and supply voltage on Delay and power dissipation.

UNIT -IV
CMOS circuit Design: CMOS logic**,** pseudo NMOS logic, pass transistor logic, Transmission Gate logic and Dynamic logic circuit design. Designing of Combinational logic circuit, sequential logic circuit design and semiconductor memory circuit.

UNIT -V
Layout: Stick diagram rules for nMOS and CMOS technology, lambda based and micron based design rules. Layout design for CMOS inverter Circuit, circuit Extraction from Layout. Limitations of CMOS in NANO scale circuit design.

BOOKS RECOMMENDED

[1] Sung-mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuit analysis and Design,* 3rd Edition, Tata McGraw-Hill.
[2] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit design, layout and Simulation*, Series Edition, PHI, IEEE press,
[3] Yuan Taur and Tak H. Ning, *Fundamentals of Modern VLSI Devices*, Special Edition, Cambridge university press,1998
[4] Neil H.E. Weste and Kamran Esharhian, *Principal of CMOS VLSI design*,2nd Edition, PHI,.

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Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Communication)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5ET556 Fuzzy Logic and Neural Network	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
To provides an understandable approach to knowledge-based systems for problem solving by combining different methods of AI, fuzzy systems, and neural networks.

Prerequisite(s):
Overview of Artificial Intelligence and Digital systems.

COURSE OF CONTENTS

UNIT -I Fuzzy Set Theory and Fuzzy System:
Fuzzy sets, operations on fuzzy sets, intersections and unions, fuzzy relations, fuzzy compositions.
Extension principle, fuzzy numbers, arithmetic operations, approximate reasoning, fuzzy inference, linguistic model of complex systems, firing of rules.

UNIT -II
Introduction to Fuzzy Control :
Fuzzy control basics, relationship to PID control, construction of knowledge base, Mamdani and Sugeno fuzzy knowledge base controls, defuzzification, fuzzy control examples, fuzzy nonlinear simulation, genetic algorithms, tuning of fuzzy systems.

UNIT -III
Introduction to Neural Networks:
What is a Neural Network. Models of a Neuron. Network Architectures. Learning Processes.

UNIT -IV
Perceptron Model and Self Organising Maps:
Unconstrained Optimization Techniques. Linear Least-Squares Filters. Least-Mean-Square Algorithm. Perceptron. Back-Propagation Algorithm. XOR Problem. Generalization. Approximations of Functions.
Self-Organizing Map algorithm. Learning Vector Quantization.

UNIT -V
Fuzzy Neural Networks
Integration of fuzzy logic and neural networks ,Fuzzy Hybrid neural, Computation of fuzzy logic inferences by hybrid neural net,Trainable neural nets for fuzzy IF-THEN rules,Implementation of fuzzy rules by regular FNN of *Type 2* ,Implementation of fuzzy rules by regular FNN of *Type 3* ,Tuning fuzzy control parameters by neural nets,Fuzzy rule extraction from numerical data,Neuro-fuzzy classifiers,ANFIS,Applications of fuzzy neural systems.

BOOKS RECOMMENDED

[1] S. Haykin, "*Neural Networks: A Comprehensive Foundation*", Prentice Hall, 1999. Reference and Reading Materials:
[2] G J Klir and T A Folger, "*Fuzzy sets, uncertainty, and information*", Prentice-Hall, 1992.
[3] D. Driankov, H. Hellendoorn and M Reinfrank, "*An introduction to fuzzy control*", Springer-Verlag, 1993.
[4] G J Klir and B Yuan, "*Fuzzy Sets and Fuzzy Logic - Theory and Applications*", Prentice-Hall, 1995.
[5] C. Bishop, "*Neural Networks for Pattern Recognition*", Oxford University Press, 1995.