Devi Ahilya University, Indore, India Institute of Engineering & Technology				**III Year B.E. (Electronics and Telecommunication Engg.)**			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
6ETRC3 SoC DESIGN USING HDL	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
	3	**1**	**2**	**3**	**1**	**1**	**5**
Duration of Theory Paper: 3 Hours							

Course Learning Objective:

The course is designed

1. To understand the basics of VLSI Design Methodologies.
2. To understand the Concept of PLD based VLSI Design on FPGA/CPLD.
3. To apply the concept of Digital design for designing basic logic cells using Verilog HDL.
4. To implement various Digital circuit/Modules through different Verilog Modelling Techniques.
5. To Understand the concept of Simulation, Synthesis and Implementation of Digital design on PLD through EDA Tool

Prerequisite(s): Digital Design, Microprocessor architecture, C++ language.

COURSE CONTENTS

UNIT –I

Overview of Digital Design with Verilog HDL -Evolution of CAD, emergence of HDLs, typical HDL-based design flow, why Verilog HDL?, trends in HDLs.

Hierarchical Modeling Concepts -Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

Basic Concepts -Lexical conventions, data types, system tasks, compiler directives.

UNIT -II

Modules and Ports-Module definition, port declaration, connecting ports, hierarchical name referencing.

Gate-Level Modeling -Modeling using basic Verilog gate primitives, description of and/or and buf/nottype gates, rise, fall and turn-off delays, min, max, and typical delays.

Dataflow Modeling -Continuous assignments, delay specification, expressions, operators,operands, operator types.

UNIT -III

Behavioral Modeling -Structured procedures, initial and always,blocking and non-blocking statements, delay control, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

Tasks and Functions -Differences between tasks and functions, declaration, invocation.

Useful Modeling Techniques -Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

UNIT -IV

Timing and Delays -Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.

Logic Synthesis with Verilog HDL-Introduction to logic synthesis, impact of logic synthesis, Verilog HDL constructs and operators for logic synthesis, synthesis design flow, verification of synthesized circuits, modeling tips, design partitioning.

UNIT -V

Introduction to SystemVerilog- SystemVerilog vs Verilog, SystemVerilog for Verification, Data types, Control Flow, SystemVerilog Threads, Communication, Interfaces,Classes, Assertion based verification.

Course Outcome:

Students earned credits will develop ability to

CO.No.	CO	PO
CO1	Design and model combinational circuits with Verilog HDL at different levels.	PO-1,PO-2
CO2	Design and analyse various sequential digital circuits by Verilog HDL	PO-1,PO-2
CO3	Understand the different Modelling styles, Functions ,Tasks and advance designing for PLD	PO-1, PO-2, PO-3, PO-5
CO4	Analyse different types of FPGAs and their modules	PO-1, PO-2, PO-3, PO-5
CO5	Understand the Project/Module Design using Xilinx FPGA board	PO-1, PO-2, PO-3, PO-5

CO-PO Relationship

CO	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12
CO1	3	3										
CO2	2	2	1									
CO3	2	2	1		2							
CO4	2	2	1		2							
CO5	2	2	1		2							

BOOKS RECOMMENDED

[1] Samir Palnitkar , "Verilog HDL-A guige to Digital Design and Synthesis " 2nd Edition, Pearson , 2006.
[2] J. Bhaskar, "A Verilog HDL Primer", B.S Publications,
[3] Douglas J. Smith, "Hdl Chip Design : A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VERILOG or Verilog".Doone Pubns ,1998.
[4] Blaine Readler , "Verilog by Example: A Concise Introduction for FPGA Design", Full Arc Press, 2011

List of Practical Assignments/Experiments:

Note: For Q1 to Q6 use behavioral modeling. For Q7 to Q8 use data flow modeling and for Q8 to Q14 use structural modeling.

Q.1 Write and simulate a VERILOG code for a Full Adder.

Q.2 Write and simulate a VERILOG code for 8X1 Multiplexer using if-elseif statement, case statement and nested if statement.

Q.3 Write and simulate a VERILOG code for a 3X8 decoder using case statement.

Q.4 Write and simulate a VERILOG code for a R-S Latch.

Q.5 Write and simulate VERILOG code for a J-K flip-flop triggered at falling edge of clock pulse. Also include clear and reset pins synchronized with clock pulse.

Q.6 Write and simulate VERILOG code for a synchronous 3-bit binary up-down counter. Include a selection line for selecting the mode of counting upwards or downwards.

Q.7 Design and simulate a combinational circuit with three inputs x, y, and z and three outputs A,B and C. when the binary input is 0,1,2, or 3 the binary output is one greater than the input otherwise the binary output is one less than the input.

Q.8 Write and simulate a VERILOG code for a 3-bit binary code to 3-bit grey code conversion.

Q.9 Design and simulate a 2X1 multiplexer using basic gates.

Q.10 Design and simulate a 4-bit ripple counter using T-Flip flop as basic component.

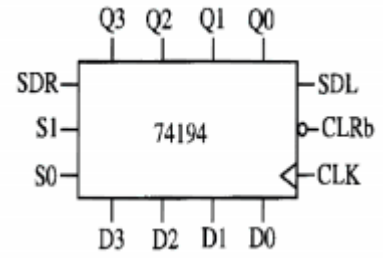
Q.11 Design and simulate a 4-bit Magnitude comparator using 1-bit Magnitude comparator as basic entity.

Q.12 Design and simulate a circuit of a 3-bit parity generator and the circuit of a 4-bit parity checker using an odd parity bit.

Q.13 Design and Simulate a 4-bit adder using 1-bit adder as basic entity.

Q.14 Design and simulate a 5X32 decoder using 3X8 and 2X4 decoder as basic entity.

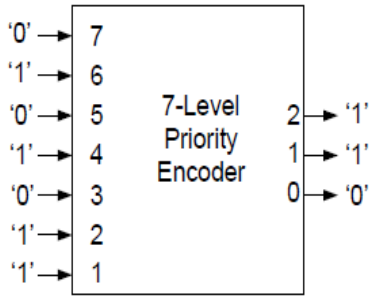
Q.15 Consider the IC74194 , 4-bit bidirectional shifter whose description is as follows: The CLRb input is asynchronous and active low and overrides all control inputs. All other state changes occur following the rising edge of the clock. If the control input S1=S0=1, the register is loaded in parallel. If S1=1 and S0=0, the register is shifted right and SDR (serial data right) is shifted into Q3.If S1=0 and S0=1, the register is shifted left and SDL (serial data left) is shifted into Q0. If S1=S0=0, no action occurs. Write the behavioral VERILOG model for the IC74194.



Q.16 Write and simulate a VERILOG behavioral model of the circuit whose truth table is given below. Here ‘X’ represents don’t care condition.

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Q.17 Write and simulate a 7-level priority encoder. The block diagram for a 7-level encoder is shown in Fig. below (7 = highest priority). The circuit must produce a 3-bit number that corresponds to the position of the active bit that has the highest priority. For example, if the input bits are "0101011" as shown in Fig. 1, then the output bits should be "110" to indicate that 6 is the highest bit position that is active. "000" should indicate that there is no active bit (all input bits are 0's).



Q.18 Write and Simulate the VERILOG structural code for 2 bit Multiplier as shown below.