Devi Ahilya University, Indore, India **Institute of Engineering & Technology**				**II Year B.E. (Information Technology)**			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
3RIPC4	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
Computer Organization & Architecture	**2**	**1**	**0**	**2**	**1**	**0**	**3**
Duration of Theory Paper: 3 Hours							

Learning Objectives:

- Provide a framework for understanding the fundamentals of computing.
- To familiarize students with relationship between hardware and software to focus on the concepts that are the basis for current computers.
- Develop skills to understand how to design a computer.
- Develop ability to understand how to enhance performance of a computer system.

Course Outcomes (COs)

CO No.	**Course Outcome**	**Program Outcomes (PO)**
CO1	Theoretical Foundations - Understand the theoretical foundations of computer organization and architecture, including the difference between organization and architecture, and the evolution of computer performance.	PO1, PO2, PO12
CO2	Memory Systems - Gain knowledge of various memory systems, including RAM, ROM, Cache, and Virtual memory, and their performance considerations.	PO1, PO2, PO4
CO3	Processing Unit - Understand the components and functions of the processing unit, including addressing modes, data path architecture, and state machines.	PO1, PO2, PO3, PO12
CO4	Input/Output Organization - Learn about I/O devices, their reliability, performance, and the interfacing with processors and memory.	PO1, PO3, PO4, PO10
CO5	Pipelining and Multiprocessors - Comprehend the principles of pipelining, multiprocessors, and modern parallel processing architectures, including GPUs.	PO1, PO2, PO3, PO5, PO10, PO12

PO-CO Matrix

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2										2
CO2	3	2		2								
CO3	3	2	3									2
CO4	3		2	2						2		
CO5	3	2	3		2					2		3

Prerequisites: Knowledge of Digital Electronics and Computer Programming.

COURSE CONTENTS

Unit-I

Introduction: Difference Between Computer Organization and Computer Architecture, Computer Types, Flynn's Classification, Functional Units, Basic Operational Concepts: Bus Structures, Software; Performance: Processor Clock, Basic Performance Equation, Clock Rate, Compiler, Performance Measurement; Multiprocessors and Multicomputers, Historical Perspective: Generation of computer, Evolution of Performance; Arithmetic for Computers: Addition and Subtraction of Signed Numbers, Multiplication of Positive Numbers, Booth Algorithm, Floating Point Arithmetic: Addition and Multiplication.

Unit-II

Memory System: Basic Concepts, Semiconductor RAM Memories, Read-Only Memories: ROM, PROM, EPROM, EEPROM, Flash Memory; Memory Speed, Size and Cost Considerations; Cache Memories: Mapping Functions, Replacement Algorithms, Performance Considerations, Hit Rate and Miss Penalty, Caches on the Processor Chip; Virtual Memories: Address Translation; Memory Management Requirements.

Unit-III

Processing Unit: Addressing Modes, Connections between the Processor and the Memory, Processor Activity, Instruction cycle, John Von Neumann Architecture, State Machine Concept, Processor as a State Machine, Data Path Architecture, Data Path Controller: Microprogrammed; Hardwired Design, Firmware Design, Microcontroller Design, Design of Flip-Flop to understand the Design of CPU.

Unit-IV

Input Output Organization: I/O Devices: Introduction**,** Typical Collection, Diversity; Dependability, Reliability, Availability, Disk Storage, Flash Storage, Connecting Processor Memory and I/O Devices, Connection Basics, Interfacing I/O Devices to the Processor Memory and Operating System: Giving Commands to I/O Devices, Communicating with the Processor, Interrupt Priority Levels, Transferring the Data between a Device and Memory, Direct Memory Access and the Memory System; I/O Performance Measures, Impact of I/O on System Performance.

Unit-V

Pipelining & Multiprocessors: Principles of Pipelining, Principles of Linear Pipelining, Clock Period, Speedup, Efficiency, Throughput, Classification of Pipeline Processor, General Pipelines and Reservation Tables, Collision Vector, State Diagram for a Pipeline, Pipeline Hazards, Shared Memory Multiprocessors, Clusters and Other Message-Passing Multiprocessors, Introduction to Graphics Processing Units, Introduction to Multiprocessor Network Topologies.

Learning Outcomes:

1. Upon completing the course, students will be able to:
2. Acquire advance knowledge and understanding of computing.
3. Use skills in computer design.
4. Apply acquired knowledge to improve performance of a computer.
5. In addition to development in technology student will be able to innovate in the architecture of computers, such as the use of caches and pipelining.
6.

Books Recommended:

1. Computer Organization, 5th Ed., C. Hamacher, Z. Vranesic, S. Zaky, McGraw Hill International Edition 2002.

2. Computer Organization and Design, 5th Ed. ,David A. Patterson, John L. Hennessy, The hardware/software interface, Morgan Kaufmann Publisher, 2014.
3. Patterson & Hennessy, Computer Organization and Design, Morgan Kaufmann Publisher, 2007.
4. Computer Architecture and Parallel Processing, Kai Hwang, Faye A. Briggs, McGraw Hill Education, 2012.

List of Assignments (Theory): During the learning of course, students need to do assignments:

1. Performance measurement of a Computer.
2. Arithmatic for Computers.
3. Cache Hit Rate/Miss Penalty issues.
4. Virtual Memory : Address Translation.
5. Use of Addressing Modes.
6. Study on designs of CPU.
7. Secondary storage performance.
8. Impact of I/O on system performance.
9. Pipelining performance.
10. Multi-core, GPU Processor and Multiprocessor : A Comparison.